

**AMENDMENTS TO THE CLAIMS**

1. (Currently Amended) An LCD device, comprising:

a LCD panel;

a plurality of source drivers applying data signals to the LCD panel;

a plurality of gate drivers applying gate driving signals to the LCD panel;

a timing controller outputting to each source driver at least two clock signals having different phases, the timing controller separately outputting R/G/B data synchronized with each clock signal to each source driver; and

at least two data buses transmitting the data separately output from the timing controller to the respective source drivers, respectively;

wherein the at least two data buses are connected between the timing controller and the respective source drivers, a number of the data buses are in proportion to a number of clock signals output from the timing controller, and the source drivers separately sample the data to thereby reduce electricity consumption.

2. (Cancelled)

3. (Previously Presented) The LCD device as claimed in claim 1, wherein the timing controller outputs the data synchronized with a rising edge time of each clock signal.

4. (Previously Presented) The LCD device as claimed in claim 1, wherein the timing controller outputs the data synchronized with a falling edge time of each clock signal.

EHC/RJW:tm

5. (Original) The LCD device as claimed in claim 1, wherein the timing controller outputs first and second clock signals having opposite phases to each other.

6. (Original) The LCD device as claimed in claim 1, wherein the timing controller outputs first, second and third clock signals, each having different phases to each another.

7. (Original) The LCD device as claimed in claim 4, wherein the source driver samples data in the falling edge time when the data synchronized with the rising edge time is output.

8. (Original) The LCD device as claimed in claim 5, wherein the source driver samples data in the rising edge time when the data synchronized in the falling edge timing is output.

9. (Previously Presented) The LCD device as claimed in claim 5, wherein odd numbered display data is output synchronized with a rising edge of the first clock signal, and even numbered display data synchronized with a rising edge of the second clock signal is output.

10. (Previously Presented) The LCD device as claimed in claim 6, wherein data for displaying R color is output synchronized with a rising edge of the first clock signal, data for displaying G color is output synchronized with a rising edge of the second clock signal, and data for displaying B color is output synchronized with a rising edge of the third clock signal.

11. (Previously Presented) A method for driving an LCD device having a timing controller transmitting digital data received from a system to each source driver, comprising the steps of:

providing a timing controller and a plurality of source drivers;

outputting from the timing controller at least two clock signals having different phases to each source driver; and

separately outputting from the timing controller the digital data to each source driver through both of at least two data buses, the digital data being synchronized with respective clock signals per odd/even numbered data or R/G/B display data,

wherein the at least two data buses are connected between the timing controller and each source driver, respectively, a number of the data buses are in proportion to a number of clock signals output from the timing controller, and the source drivers separately sample the digital data to thereby reduce electricity consumption

12. (Previously Presented) The method as claimed in claim 11, wherein the digital data is synchronized with a rising edge of each clock signal.

13. (Previously Presented) The method as claimed in claim 12, wherein each source driver samples the digital data synchronized with a falling edge of each clock signal if the digital data is output synchronized with the rising edge of each clock signal.

14. (Previously Presented) The method as claimed in claim 11, wherein the digital data is output synchronized with a falling edge of each clock signal.

15. (Previously Presented) The method as claimed in claim 14, wherein each source driver samples the digital data synchronized with a rising edge of each clock signal if the digital data is output synchronized with the falling edge of each clock signal.

16. (Previously Presented) The method as claimed in claim 11, wherein two clock signals having different phases are used when the digital data is separately output according to odd and even numbered data, and three clock signals having different phases are used when the data is separately output according to R/G/B data.

17-18. (Cancelled)

19. (Previously Presented) The LCD device as claimed in claim 1, wherein the at least two data buses are separated from each other.

20. (Previously Presented) The method as claimed in claim 11, wherein the at least two data buses are separated from each other.